Joseph Lee Greathouse, Ph.D. — Curriculum Vitae

Contact Information

Advanced Micro Devices, Inc.
7171 Southwest Pkwy.
Austin, TX 78735 USA

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WWW: www.computermachines.org

Research Interests

I like making hardware do new and potentially unintended things. Hardware performance monitors and on-chip firmware can yield intriguing data with a few well-placed tweaks.

Beyond that, power, energy, and thermal optimizations present a plethora of unsolved problems. Heterogeneous processors add an interesting dimension, as different styles of cores must share thermal and power infrastructure. I am interested in finding good local and global optimization strategies.

My Ph.D. dissertation focused on hardware methods for accelerating software analyses such as data race detectors and memory checkers. I used existing hardware, like performance counters, for this in addition to designing new hardware mechanisms.

Professional Experience

Advanced Micro Devices, Inc., Austin, TX USA

Senior Member of Technical Staff — **July 2016 – Present**

- I am currently a performance architect in the Radeon Open Compute team, where I work on optimizing our GPU software, firmware, and hardware in order to meet the demands of our GPU compute customers.
- I previously worked at AMD Research, studying performance and power monitoring, estimation, and management mechanisms for CPUs and GPUs as part of AMD's exascale program.

Member of Technical Staff — **July 2014 – June 2016**

- As part of AMD's FastForward 2 research, I worked on: high-level processor and node simulation; power analysis, modeling and control; and heterogeneous algorithms.
- This included extensions to the high-level simulation platforms I worked on throughout the FastForward program, as well as new algorithms such as described in our HiPC'15 and USENIX'16 papers.

Senior Design Engineer — **August 2012 – June 2014**

- Created a performance and power simulator for AMD's FastForward program based on analytic scaling of real hardware measurements.
- Designed CPU and GPU power monitoring, estimation, and management tools and algorithms.
- Worked with exascale proxy applications to formulate new GPGPU algorithms for AMD GPUs and APUs.

University of Michigan, Ann Arbor, MI USA

Graduate Student Research Assistant — **May 2007 – August 2012**

- Identified methods of accelerating software analyses and distributing them across many users in order to find more bugs across the user population.
- Managed graduate and undergraduate students through the development of prototype systems and writing multiple published academic papers.

Kelly IT Services / Intel Corporation, Champaign, IL USA

Research Contractor **May 2010 – Oct. 2010**

- Devised algorithmic approaches for improving the speed and accuracy of the Intel Inspector XE data race detector.
- Utilized unique performance monitoring features on Intel processors to yield orders-of-magnitude performance gains for this tool.

International Business Machines Corporation, Rochester, MN USA

Speed Team Intern **May 2008 – Aug. 2008**

- Designed and constructed an InfiniBand compliance verification suite for the IBM Galaxy-2 host channel adapter.
- Added the suite into the IBM PowerVM I/O firmware development process and found multiple bugs.

Education

University of Michigan, Ann Arbor, Ann Arbor, MI USA

Ph.D., Computer Science and Engineering, May 2012

- Thesis Topic: *Hardware Mechanisms for Distributed Dynamic Software Analysis*
- Advisor: Professor Todd Austin

M.S.E., Computer Science and Engineering, May 2008

- Concentration: Hardware Systems
- GPA: 7.73/9.0 (Rackham Scale) / 3.79/4.0 (Traditional Scale)

University of Illinois at Urbana-Champaign, Champaign, IL USA

B.S., Computer Engineering, May 2006

- With Honors
- Minor in International Engineering – Japanese
- GPA: 3.71/4.0

Conference Publications

Xudong An, Manish Arora, Wei Huang, William C. Brantley, Joseph L. Greathouse
"3D Numerical Analysis of Two-Phase Immersion Cooling for Electronic Components"
Published in the *Proceedings of the 17th IEEE Intersociety Conference on Thermomechanical Phenomena in Electronic Systems* (**ITherm 2018**), May, 2018.

Nicholas Malaya, Shuai Che, Joseph L. Greathouse, René van Oostrum, Michael J. Schulte
"Accelerating Matrix Processing with GPUs"
Published in the*Proceedings of the 24th IEEE Symposium on Computer Arithmetic* (**ARITH 24**), July, 2017.

Marko Ščrbak, Joseph L. Greathouse, Nuwan Jayasena, Krishna Kavi
"DVFS Space Exploration in Power Constrained Processing-in-Memory Systems"
Published in the *Proceedings of the 30th International Conference on Architecture of Computing Systems* (**ARCS 2017**), April, 2017.

Abhinandan Majumdar, Leonardo Piga, Indrani Paul, Joseph L. Greathouse, Wei Huang, David H. Albonesi
"Dynamic GPGPU Power Management using Adaptive Model Predictive Control"
Published in the *Proceedings of the 23rd IEEE Symposium on High Performance Computer Architecture* (**HPCA 2017**), February, 2017.

Thiruvengadam Vijayaraghavan, Yasuko Eckert, Gabriel H. Loh, Michael J. Schulte, Mike Ignatowski, Indrani Paul, Bradford M. Beckmann, Steven K. Reinhardt, William C. Brantley, Joseph L. Greathouse, Onur Kayiran, Matthew Poremba, Wei Huang, Arun Karunanithi, Greg Sadowski, Vilas Sridharan, Steven E. Raasch, Mitesh Meswani
"Design and Analysis of an APU for Exascale Computing"
Published in the *Proceedings of the 23rd IEEE Symposium on High Performance Computer Architecture* (**HPCA 2017 Industry Track**), February, 2017.

Christopher Erb, Mike Collins, Joseph L. Greathouse
"Dynamic Buffer Overflow Detection for GPGPUs"
Published in the *Proceedings of the 2017 IEEE/ACM International Symposium on Code Generation and Optimization* (**CGO 2017**), February, 2017.

Vignesh Adhinarayanan, Indrani Paul, Joseph L. Greathouse,
Wei Huang, Ashutosh Pattnaik, Wu-chun Feng
"Measuring and Modeling On-Chip Interconnect Power on Real Hardware"
Published in the *Proceedings of the 2016 IEEE International Symposium on Workload Characterization* (**IISWC 2016**), September, 2016.
Awarded Best Paper

Alex D. Breslow, Dong Ping Zhang, Joseph L. Greathouse,
Nuwan Jayasena, Dean M. Tullsen
"Horton Tables: Fast Hash Tables for In-Memory Data-Intensive Computing "
Published in the *Proceedings of the 2016 USENIX Annual Technical Conference* (**USENIX ATC '16**), June, 2016.

Mayank Daga, Joseph L. Greathouse
"Structural Agnostic SpMV: Adapting CSR-Adaptive for Irregular Matrices"
Published in the *Proceedings of the 2015 IEEE International Conference on High Performance Computing* (**HiPC 2015**), December, 2015.

Abhinandan Majumdar, Gene Wu, Kapil Dev, Joseph L. Greathouse, Indrani Paul,
Wei Huang, Arjun Karthik Venugopal, Leonardo Piga, Chip Freitag, Sooraj Puthoor
"A Taxonomy of GPGPU Performance Scaling"
Published in the *Proceedings of the 2015 IEEE International Symposium on Workload Characterization* (**IISWC 2015**), October, 2015.

Gene Wu, Joseph L. Greathouse, Alexander Lyashevsky, Nuwan Jayasena, Derek Chiou
"GPGPU Performance and Power Estimation Using Machine Learning"
Published in the *Proceedings of the 21st IEEE Symposium on High Performance Computer Architecture* (**HPCA 2015**), February, 2015.

Bo Su, Junli Gu, Li Shen, Wei Huang, Joseph L. Greathouse, Zhiying Wang
"PPEP: Online Performance, Power and Energy Prediction Framework and DVFS Space Exploration"
Published in the *Proceedings of the 47th Annual IEEE/ACM International Symposium on Microarchitecture* (**MICRO-47**), December, 2014.

Joseph L. Greathouse, Mayank Daga
"Efficient Sparse Matrix-Vector Multiplication on GPUs using the CSR Storage Format"
Published in the *Proceedings of the International Conference on High Performance Computing, Networking, Storage and Analysis* (**SC14**), November, 2014.

Dong Ping Zhang, Nuwan Jayasena, Alexander Lyashevsky, Joseph L. Greathouse,
Lifan Xu, Michael Ignatowski
"TOP-PIM: Throughput-Oriented Programmable Processing in Memory"
Published in the *Proceedings of the 23rd International Symposium on High Performance*

Parallel and Distributed Computing (**HPDC '14**), June, 2014.
Nominated for Best Paper

Bo Su, Joseph L. Greathouse, Junli Gu, Michael Boyer, Li Shen, Zhiying Wang
"Implementing a Leading Loads Performance Predictor on Commodity Processors"
Published in the *Proceedings of the 2014 USENIX Annual Technical Conference* (**USENIX ATC '14**), June, 2014.

Andrea Pellegrini, Joseph L. Greathouse, Valeria Bertacco
"Viper: Virtual Pipelines for Enhanced Reliability"
Published in the *Proceedings of the 39th Annual International Symposium on Computer Architecture* (**ISCA 2012**), June, 2012.

Joseph L. Greathouse, Hongyi Xin, Yixin Luo, Todd Austin
"A Case for Unlimited Watchpoints"
Published in the *Proceedings of the 17th International Conference on Architectural Support for Programming Languages and Operating Systems* (**ASPLOS 2012**), March, 2012.

Joseph L. Greathouse, Zhiqiang Ma, Matthew I. Frank, Ramesh Peri, Todd Austin
"Demand-Driven Software Race Detection using Hardware Performance Counters"
Published in the *Proceedings of the 38th Annual International Symposium on Computer Architecture* (**ISCA 2011**), June, 2011.

Joseph L. Greathouse, Chelsea LeBlanc, Todd Austin, Valeria Bertacco
"Highly Scalable Distributed Dataflow Analysis"
Published in the *Proceedings of the 9th Annual IEEE/ACM International Symposium on Code Generation and Optimization* (**CGO 2011**), April, 2011.
Awarded Best Student Presentation

Joseph L. Greathouse, Ilya Wagner, David A. Ramos, Gautam Bhatnagar, Todd Austin, Valeria Bertacco, Seth Pettie
"Testudo: Heavyweight Security Analysis via Statistical Sampling"
Published in the *Proceedings of the 41st Annual IEEE/ACM International Symposium on Microarchitecture* (**MICRO-41**), November, 2008.

Workshop Publications

Christopher Erb, Joseph L. Greathouse
"clARMOR: A Dynamic Buffer Overflow Detector for OpenCL Kernels
Published in the Proceedings of the International Workshop on OpenCL (**IWOCL 2018**), May, 2018.

Joseph L. Greathouse, Kent Knox, Jakub Poła, Kiran Varaganti, Mayank Daga
"clSPARSE: A Vendor-Optimized Open-Source Sparse BLAS Library"
Published in the Proceedings of the International Workshop on OpenCL (**IWOCL 2016**), April, 2016.

Yingying Tian, Sooraj Puthoor, Joseph L. Greathouse, Bradford M. Beckmann, Daniel Jiménez
"Adaptive GPU Cache Bypassing"
Published in the Proceedings of the 8th Workshop on General Purpose Processing on GPUs (**GPGPU-8**), February, 2015.

Adam McLaughlin, Indrani Paul, Joseph L. Greathouse, Srilatha Manne, Sudhakar Yalamanchili
"A Power Characterization and Management of GPU Graph Traversal"
Published at the Fourth Workshop on Architectures and Systems for Big Data (**ASBD 2014**), June, 2014.

Joseph L. Greathouse, Alexander Lyashevsky, Mitesh Meswani, Nuwan Jayasena, Michael Ignatowski
"Simulation of Exascale Nodes through Runtime Hardware Monitoring"
Published at the Workshop on Modeling & Simulation of Exascale Systems & Applications (**ModSim 2013**), September, 2013.

Dong Ping Zhang, Nuwan Jayasena, Alexander Lyashevsky, Joseph L. Greathouse, Mitesh Meswani, Mark Nutter, Michael Ignatowski
"A New Perspective on Processing-in-memory Architecture Design"
Published at the ACM SIGPLAN Workshop on Memory Systems Performance and Correctness (**MSPC 2013**), June, 2013.

Joseph L. Greathouse, Todd Austin
"Position Paper: The Potential of Sampling for Dynamic Analysis"
Published in the *Proceedings of the 6th ACM SIGPLAN Workshop on Programming Languages and Analysis for Security* (**PLAS 2011**), June, 2011.

Software Projects

AMD Research Instruction Based Sampling Toolkit
`https://github.com/jlgreathouse/AMD_IBS_Toolkit`

clSPARSE – A Vendor-Optimized Sparse BLAS Library for GPUs Using OpenCL
`https://github.com/clMathLibraries/clSPARSE`

clARMOR – A Buffer Overflow Detector for OpenCL GPU Kernels
`https://github.com/ROCm-Developer-Tools/clARMOR`

Patents

Mayank Daga, Joseph L. Greathouse
"Efficient Sparse Matrix-Vector Multiplication on Parallel Processors"
U.S. Patent Number 9,697,176, Granted July 4, 2017.

Joseph L. Greathouse, David S. Christie
"Randomly Branching Using Hardware Watchpoints"
U.S. Patent Number 9,483,379, Granted November 1, 2016.

Joseph L. Greathouse, David S. Christie
"Randomly Branching Using Performance Counters"
U.S. Patent Number 9,448,909, Granted September 20, 2016.

Joseph L. Greathouse, Anton Chernoff
"User-level Hardware Branch Records"
U.S. Patent Number 9,372,733, Granted June 21, 2016.

Presentations

"Accelerating Dynamic Software Analyses"
Microsoft Research, Feb. 23, 2012.

"On-Demand Dynamic Software Analysis"
AMD Tech Topics Series, Dec. 12, 2011.

"Hardware Support for On-Demand Software Analysis"
University of Michigan CSE Graduate Student Honors Competition, Dec. 8, 2011.

"Accelerating Dynamic Software Analyses"
Microsoft Research Silicon Valley, Dec. 2, 2011.

"Accelerating Dynamic Software Analyses"
VMware, Dec. 1, 2011.

"On-Demand Dynamic Software Analysis"
Intel Labs, Nov. 29, 2011.

"Sampling Dynamic Dataflow Analyses"
University of British Columbia Computer Science Department, June 10, 2011.

Posters

"Scalable Security Vulnerability Analysis via Sampling"
Presented at the 2011 GSRC Annual Symposium, Nov. 16, 2011.

"Testudo: Heavyweight Security Analysis via Statistical Sampling"
Presented at the 2008 University of Michigan Engineering Graduate Symposium, Nov. 7, 2008

Teaching Experience

University of Michigan, Ann Arbor, Ann Arbor, MI USA

Graduate Student Instructor **Jan. 2012 – Apr. 2012**
EECS 570: Parallel Computer Architecture

- Responsible for guiding multiple graduate student research projects related to parallel computing.
- Set up software infrastructure for assignments on parallel programming and cache coherency protocols.

University of Illinois at Urbana-Champaign Champaign, IL USA

Undergraduate Teaching Assistant **Jan. 2005 – Aug. 2006**
ECE 290: Computer Engineering I

- Graded homework assignment and tests for four semesters.
- Taught discussion section for this undergraduate digital logic course during the summer of 2006.

Grader **Aug. 2005 – Dec. 2005**
CS 433: Computer System Organization

- Graded homework assignment for this undergraduate computer architecture course.

Professional Activities

Program committee member for ISPASS (2015), HPPAC (2015–2018)
External reviewer for MICRO (2009, 2013, 2014, 2017), HPCA (2013, 2014), IEEE CAL (2015-2017), IEEE TPDS (2017), IEEE TCAD (2017, 2018), IEEE TMSCS (2018), SC (2017), SRCS (2013), FMCAD (2010), and MPDI Computation (2018)
External reviewer (through Todd Austin) for ASPLOS (2012, 2013), CODES (2011), DATE (2008–2012), FMCAD (2010), HPCA (2009, 2010, 2012), ISCA (2009, 2010, 2012), MICRO (2008, 2011, 2012), and PACT (2012)
Judge for SRC TechCon (2015)
Senior Member, ACM
Member, IEEE
UM Advanced Computer Architecture Laboratory Reading Group organizer (2009–2010), compute cluster administrator (2008–2011)

Awards and Honors

IISWC 2016 Best Paper Award
2011 University of Michigan CSE Graduate Student Honors Competition 1st Place
CGO 2011 Best Student Presentation Award
University of Michigan EECS Departmental Fellowship, 2006–2007
Eta Kappa Nu Electrical and Computer Engineering Honor Society
Tau Beta Pi Engineering Honor Society
Illinois Chancellor's Scholar
Illinois Engineering James Scholar

Skills

Programming Languages:

- C, C++, OpenCL, x86 assembly, AMD GCN assembly, Python

Software Systems:

- Linux, Xen, and Solaris kernel internals, QEMU emulator internals, USB firmware programming, Intel Pin dynamic binary instrumenation tool design, and multiple AMD-internal simulation, firmware, and analysis tools